UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/672,395 | 09/28/2000 | Paul Lap Tak Cheng | 0325.00370 | 8271 |

21363 7590 09/22/2003

CHRISTOPHER P. MAIORANA, P.C.
24025 GREATER MACK
SUITE 200
ST. CLAIR SHORES, MI 48080

| EXAMINER | |
|---|---|
| TRUJILLO, JAMES K | |
| ART UNIT | PAPER NUMBER |
| 2185 | |

DATE MAILED: 09/22/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/672,395 | CHENG ET AL. | |
| | Examiner | Art Unit | |
| | James K. Trujillo | 2185 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *22 January 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 September 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

1. The office acknowledges the receipt of the following and placed of record in the file: IDS dated 1/28/01.

2. Claims 1-20 are presented for examination.

### *Drawings*

3. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

4. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore the third signal having a first duration in response to said second signal and a second duration when generated in response to the expiration of said predetermined time period as per claim 14 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

### *Claim Rejections - 35 USC § 103*

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-4, 6-14, 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rosno et al., U.S. Patent 6,535,986 (hereinafter Rosno) in view of Pole, II et al., U.S. Patent 6,311,281 (hereinafter Pole) and Applicant's admitted prior art (hereinafter AAPA).

7. As to claim 1, Rosno substantially teaches, as per claim 1, an apparatus comprising a circuit configured to:

> change a frequency of one or more first signals (clock signals from PLL, DM, SCC 120 to the clock distribution 130 and finally to chip logic-memory latches) in response to a second signal (signal output from State Machine 160 to Chip Frequency Synthesizer 110) [figure 1 and corresponding text].

Rosno does not expressly disclose generating a third signal in response to either said second signal or a predetermined time expiring.

Specifically, the apparatus of Rosno changes the frequency of a plurality of clock signal to adjust the clocking system of a digital computer. Ronso does this by starting the system at a default frequency then automatically incrementing the frequency and rerunning tests until a failure occurs. These steps are repeated until a desired timing margin and frequency of the clock is achieved [col. 3 lines 39-65 and figure 2].

Pole teaches an apparatus that generates a third signal (reset for a processor) in response to another signal (change of frequency) [col. 2 lines 16-21].

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Rosno by generating the third signal (the reset) in response to the second signal (Chip Frequency Synthesizer output signal) as taught by Pole because all systems are directed toward changing the frequency of a processor. An artisan would have been motivated to make the modification because Pole teaches that resetting the processor is necessary for the desired on-the-fly change of frequency that allows for a desired quick change in performance level [col. 2 lines 16-34]. These features are also desirable in Rosno. This modification results in the claimed invention.

AAPA teaches that if the frequency of a programmable clock circuit changes faster thatn the microprocessor can track the microprocessor will hang. AAPA further teachea a conventional apparatus used in recovering a system from a failure, such as a hang, by generating a third signal (a reset for resetting the microprocessor) in response to a predetermined time period expiring using a watchdog timer in the case of a hang [page 2 line 1 through page 3 line 2].

It would have been obvious to one of ordinary skill in the art at the time of the invention to further modify Rosno combined with Pole by incorporating the apparatus taught by AAPA to recover from a failure because both systems are directed toward recovering a system from a failure. The modification would be made by adding a watchdog timer using a predetermined time period to reset the microprocessor of Rosno when a failure occurs as taught by AAPA. The reset would occur with the frequency prior to the failure. An artisan would have been motivated to make the modification because the modification would ensure that the system of Rosno would

continue repeat the steps of adjusting the frequency especially the failure which occurred hangs the system.

8. As to claim 2, Rosno combined with Pole and AAPA taught the apparatus according to claim 1 described above. Rosno further taught wherein said second signal programs said frequency [col. 5 lines 18-19].

9. As to claim 3, Rosno combined with Pole and AAPA taught the apparatus according to claim 1 described above. The combination of Rosno, Pole and AAPA does not expressly disclose wherein said one or more first signals are generated by one or more phase lock loop circuits. Specifically, Rosno discloses using one phase lock loop to generate one or first signals (clock signal is distributed to multiple devices) [col. 4 lilnes 55-59]. However, it would have been obvious to one of ordinary skill the art at the time of the invention to further modify the combination of Rosno, Pole and AAPA by incorporating more than one phase lock loop to generate the more than one first signal because the system of Rosno requires more than one first signal. An artisan would have been motivated to make to the modification because an artisan would have recognized that having more than phase lock loop is another well know and reliable way distribute clock signals in a system. Further, incorporating more than one phase lock loop does not depart from the spirit and scope of the invention of Rosno, therefore the claimed invention is not patentably distinguishable from the invention of Rosno.

10. As to claim 4, Rosno combined with Pole and AAPA taught the apparatus according to claim 3 described above. Rosno teaches wherein said signal program a single phase lock loop. According to the modification as described above it would have been obvious to one of ordinary

skill in the art at the time of the invention to make the modification to program all phase lock loops in the system to provide control of all distributed clock signals.

11. As to claim 6, Rosno combined with Pole and AAPA taught the apparatus according to claim 1 described above. AAPA further taught wherein the predetermined time period is programmable. AAPA uses a watchdog timer to reset after a preset amount of time, which implicitly teaches that the time period would be programmable. Alternatively, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Rosno combined with AAPA an Pole by using a programmable watchdog timer because they are well known and widely used in the computer art to reset a processor. An artisan would have been motivated to make such a modification because it is desirable to make the system flexible with respect to the amount of time before a reset is issued.

12. As to claim 7, Rosno combined with Pole and AAPA taught the apparatus according to claim 1 described above. Rosno combined with Pole and AAPA together do not expressly disclose wherein said predetermined time period is started in response to said second signal. However, Pole teaches that a third (reset) signal should be issued when changing the frequency (a second signal) of the system. AAPA teaches using a predetermined time period to recovery from a system hang by issuing a third (reset) signal.

It would have been obvious to one of ordinary skill in the art at the time of the invention to further modify Rosno combined with Pole and AAPA by starting the predetermined time period (as taught by AAPA) in response to the second signal (frequency adjustment), because it is desirable to reset the processor when changing the frequency as set forth hereinabove by Pole. However, an artisan would recognize that if the frequency of adjustment were such that the

processor hangs, as AAPA suggests teaches, there would be no automatic recovery, forcing user intervention. Therefore, making the modification would allow an automatic recovery (from a hang) to be enabled, desirably reducing the need for user intervention, when the predetermined time period is initiated in response to the second signal.

13. As to claim 8, Rosno combined with Pole and AAPA taught the apparatus according to claim 1 described above. AAPA further taught using a watchdog timer circuit that measures the predetermined time period [figure 1].

14. As to claim 9, Rosno combined with Pole and AAPA taught the apparatus according to claim 1 described above. Rosno further teaches wherein one of the first signals is presented to a clock input of a processor because Rosno discloses that his invention is directed toward adjusting the clock control settings at different operating frequencies [col. 2 lines 63-67]. It is inherent that adjusting different operating frequencies entails changing the clock input of a processor.

AAPA teaches wherein of the third signal would be presented to a reset input of said processor [figure 1].

15. As to claim 10, Rosno combined with Pole and AAPA taught the apparatus according to claim 9 described above. Rosno further taught wherein said second signal (clock control settings) is generated using a number of instructions executed by said processor (the state machine/service processor) [col. 5 line 18-19].

16. As to claim 11, Rosno combined with Pole and AAPA taught the apparatus according to claim 10 described above. In Rosno it is inherent that the instructions are contained in computer readable memory because they are sent from a computer (processor).

17. As to claim 12, Rosno combined with Pole and AAPA taught the apparatus according to claim 10 described above. Rosno combined with Pole and AAPA do not expressly disclose wherein said instructions are part of a basic input output system routine. However, Rosno discloses that the adjustment of the adjustment of the clock control settings using said instructions is done preferably at every initial program load [col. 6 lines 12-20]. It is well known in the computer arts that initial program loading is often by basic input output system routine. It would have been obvious to one of ordinary skill in the art at the time of the invention to further modify the combination of Rosno combined with Pole and AAPA by implementing the instructions as part of a basic input output system routine because initial program loading is often and reliably done by the basic input output system routine. An artisan would have further been motivated to make the modification because it would allow the instructions to be readily available for the initial program load with having to read them from another location reducing the time for the routine to be completed.

18. As to claim 13, Rosno combined with Pole and AAPA taught the apparatus according to claim 9 described above. Rosno combined with Pole and AAPA do not expressly disclose wherein the predetermined time period expires only when the processor hangs. It is well known in the computer arts that watchdog timers use a predetermined time period that expires only when the processor hangs. AAPA teaches using a watchdog timer to reset a processor. It would have been obvious to one of ordinary skill in the art at the time of the invention to further modify Rosno combined with Pole and AAPA by requiring the predetermined time period of the watchdog time to expire only when the processor hangs.

19. As to claim 14, Rosno combined with Pole and AAPA taught the apparatus according to claim 9 described above. Rosno combined with Pole and AAPA do not expressly disclose wherein said third signal has a first duration when generated in response to said second signal and a second duration when generated in response to the expiration of said predetermined time period. In summary, the prior art does not show the generated third signal having two different durations.

It would have been obvious to one of ordinary skill in the art at the time of the invention to further modify Rosno combined with Pole and AAPA by having a first duration for the third signal when generated in response to said second signal and for the third signal to have a second duration when generated in response to the expiration of said predetermined time period. Applicant has not disclosed that having two different durations for the third signal provides an advantage, is used for a particular purpose, or solves a stated problem. One of ordinary skill in the art, furthermore, would have expected Applicants invention to perform equally with the same durations because both signals generate a reset.

Therefore, it would have been obvious to one of ordinary skill in this art to modify Rosno combined with Pole and AAPA to obtain the invention as specified in claim 14.

20. As to claims 16 and 17, Rosno combined with Pole and AAPA taught the apparatus according to claim 1 described above. Rosno combined with Pole and AAPA does not expressly disclose wherein said circuit is configured to skew said one or more first signals.

However, Rosno discloses that one or more first signals are distributed to different logic and memory circuits using different paths. An artisan would have recognized that in distributing the one or more first signals through different paths would require skew times to be adjusted for

each path accordingly to ensure proper clocking of the system. Having programmable skew in data and clock signal paths is well known in the computer arts to ensure proper clocking of the system.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Rosno combined with Pole and AAPA by having a circuit configured to skew said one or more first signal by incorporating programmable skew or delay for each particular signal path. An artisan would have been motivated to make such a modification to ensure proper timing throughout the system ensuring data is transferred correctly.

21. As to claim 18, claim 18 is rejected on the same basis as claim 1.

22. As to claim 19, Rosno combined with Pole and AAPA taught the claimed apparatus therefore together they teach the claimed method to operate the claimed apparatus.

23. As to claim 20, Rosno combined with Pole and AAPA taught the apparatus according to claim 19 described above. Rosno combined with Pole and AAPA does not expressly disclose wherein when the processor hangs, changing said frequency of said clock signal to a fail-safe frequency and resetting said processor.

In summary, Rosno teaches changing the frequency to obtain a desired timing margin and desired frequency of said clock. In changing the frequency Rosno increases the frequency until failure. If a failure occurs, Rosno then sets the frequency and sets clock control settings [figure 2 and corresponding text]. Rosno is silent with respect to how the frequency is set after a failure. Pole teaches that after changing the frequency a reset is necessary.

It would have been obvious to one of ordinary skill in the art at the time of the invention to further modify Rosno combined with Pole and AAPA by setting the frequency, if a failure

occurred, to a fail-safe frequency. After setting the frequency the processor would be reset as taught by Pole. An artisan would have set the frequency to a fail-safe frequency because it would ensure that the processor would not fail and test would then be run to desirably find acceptable timing margin and operating frequency.

24. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rosno, Pole and AAPA as applied to claim 1 above, and further in view of Ogilvie et al., U.S. Patent 6,038,629 (hereinafter Ogilvie).

25. As to claim 5, Rosno combined with Pole and AAPA taught the apparatus according to claim 1 described above. However, Rosno combined with Pole and AAPA do not expressly teach wherein said one or more first signals are generated using a divider network. Specifically, Rosno teaches that clock signals are distributed to various logic, processor, and memory circuits. Rosno is silent with respect to how the clock signals are distributed.

Ogilvie taught an apparatus having one or more phase lock loops wherein the clock signals of one of the phase lock loops is distributed using a divider network to provide clock signals to various logic, processor and memory circuits [col. 8 lines 10-17].

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the combination of Rosno, Pole and AAPA by using a divider network as taught by Ogilvie because all necessary systems are directed toward distributing clock signals. An artisan would have been motivated to make the modification because the divider network as taught by Ogilvie would allow different clock frequencies to be distributed which would be desirable in the combination of Rosno, Pole and AAPA.

26. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Rosno, Pole and AAPA as applied to claim 1 above, and further in view of $I^2C$ Bus specification (submitted in IDS, hereinafter "the $I^2C$ Bus specification").

27. As to claim 15, Rosno combined with Pole and AAPA taught the apparatus according to claim 1 described above. Rosno combined with Pole and AAPA do not expressly wherein said circuit comprises an inter-integrated circuit interface circuit.

The $I^2C$ Bus specification teaches using an $I^2C$ Bus has many advantages [pages 4-6]. It would have been obvious to one of ordinary skill in the art at the time of the invention to further modify Rosno combined with Pole and AAPA incorporating within their circuitry an inter-integrated ($I^2C$) interface circuit. An artisan would have made the modification because the $I^2C$ Bus specification teaches that it is beneficial to use an $I^2C$ bus for coordinating data and clock signals between buses. In using an $I^2C$ Bus, an inter-integrated ($I^2C$) interface circuit would be necessary, resulting in the claimed invention.

***Conclusion***

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Pat. No. 5,751,665 to Tanoi. This patent teaches a clock distribution circuit having a plurality of phase lock loops.

Japan Pat. No. JP405055914 A to Sato. This patent teaches controlling an oscillator to reach a desired frequency.

Hegde, A., "Clock distribution in high speed system", Northcon/93, Conference Record, 12-14, Oct. 1993, Page(s): 61 -65. This paper teaches clock distribution in a computer system.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James K. Trujillo whose telephone number is (703) 308-6291. The examiner can normally be reached on M-F (7:30 am - 5:00 pm) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (703) 305-9717. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

James Trujillo
September 9, 2003

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100